Piezo Haptic Driver with Digital Front End

AWP1923

KEY FEATURES

- High-Voltage Low Power Piezo Driver
  - o Drive 100nF at 190VPP and 250Hz with 490mW
  - o Drives Capacitive Loads up to 1000nF
  - o Energy Recovery
  - o Differential Output
  - o Small Solution Footprint, QFN & WLCSP
- Low Quiescent Current: SHUTDOWN; SLEEP; IDLE; IDLE mode Current only 90uA
- Multiple operating modes: AUTOPLAY; SENSEPLAY; DIRECTPLAY; FIFOPLAY; SRAMPLAY
- Wide Supply Voltage Range of 2.3V to 5.5V
- Advanced Piezo Sensing Capabilities
  - o 8.8 mV Sensing Resolution
  - o Interrupt Generation
  - o Automatic Triggering of Haptic Feedback
- Integrated Digital Front End with I2C
  - o 1024 sample Internal FIFO Interface
  - o 1.8 V Digital I/O Supply
  - o Supports Continuous Waveforms Playback
  - o State Retention in SLEEP Mode
- Fast Start Up Time less than 200 µs
- Multi-Actuator Synchronization; address selection; Power-on-Reset
- ESD verification pass, latch up verification pass

APPLICATIONS

- Mobile Phones and Tablets
- Portable Computers, Keyboards and Mice
- Gaming Controllers, Wearables
- Electronic Cooling

GENERAL DESCRIPTION

The AWP1923 is a single-chip piezo actuator driver with energy recovery. It can drive actuators with waveforms up to 190 Vpk-pk while operating from a 2.3 to 5.5 V supply voltage. Its low power and small size make it ideal for applications requiring minimal power consumption. The AWP1923 features high-resolution piezo sensing capabilities allowing haptic feedback to be automatically played when detection conditions are met.

The AWP1923 differential driver achieves low distortion waveforms and quiet actuator operation. All settings are adjustable through the digital front end to reduce the BOM. Data and configuration parameters are easily communicated to the AWP1923 through its two wire I2C interface. A flexible deep FIFO enables the streaming of digital waveform data for playback or the transmission of burst data for more bandwidth efficiency. The AWP1923 also integrates 1.5 kB of RAM waveform memory to generate waveforms with minimal communication bandwidth.

A dedicated SYNC pin can synchronize multiple AWP1923 controllers to simultaneously drive multiple actuators within 2µs. In addition to SYNC synchronization, AWP1923 can also support CLK_SYNC synchronization. This function synchronizes the clock, and multiple chips share the same clock.

With a typical start-up time of less than 200µs, the AWP1923 latency is negligible in most systems. Various safety systems protect the AWP1923 from damage in case of a fault.

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TYPICAL APPLICATION

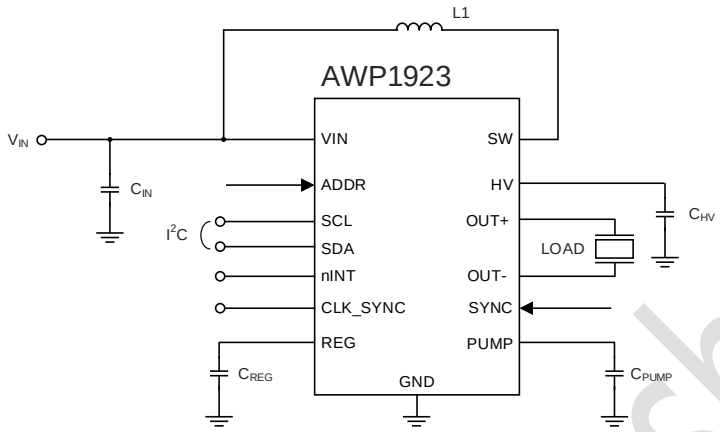

Figure 1. Typical Application Circuit

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PIN CONFIGURATION

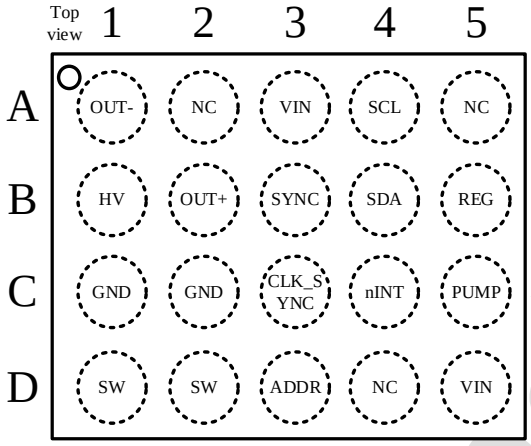

*Figure 2. WLCSP 2.1mm*1.7mm 20B package (TOP VIEW; NOT TO SCALE)*

Table 1. WLCSP 20B Pin Function Descriptions

Pin No.	Pin Name	Type(1)	Description
A1	OUT-	O	Negative Differential Output
A2	NC	-	No connect
A3	VIN	P	Main Power Supply
A4	SCL	I	I2C clock
A5	NC	-	No connect
B1	HV	P	High-Voltage Output
B2	OUT+	O	Positive Differential Output
B3	SYNC	I/O	1.Synchronization pin;2.Positive Input of ATOA(I/O)
B4	SDA	I/O	I2C data
B5	REG	P	Internal 1.8 V Regulator Output
C1	GND	P	Ground
C2	GND	P	Ground
C3	CLK_SYNC	I/O	CLK Synchronization Pin, Can Be Set to Either Master or Slave Mode
C4	nINT	O	1.Interrupt or Alarm Out Pin;2. Negative Input of ATOA(O)
C5	PUMP	P	Internal 2.2 V Regulator Output Analog Power
D1	SW	P	Internal Power Converter Switch Pin
D2	SW	P	Internal Power Converter Switch Pin
D3	ADDR	I	IIC Slave Address.
D4	NC	-	No connect
D5	VIN	P	Main Power Supply

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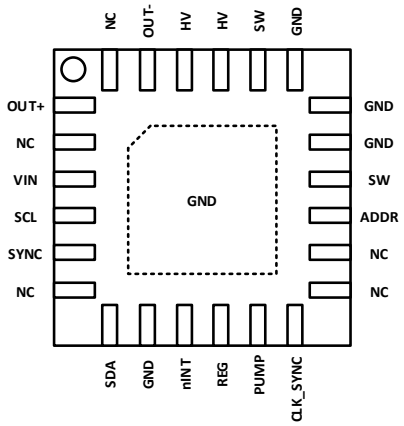

*Figure 3. QFN 4mm*4mm 24L package with exposed thermal pad (TOP VIEW; NOT TO SCALE)*

Table 2. QFN24L Pin Function Descriptions

Pin No.	Pin Name	Type(1)	Description
1	OUT+	O	Positive Differential Output(O)
2	NC	-	No connect
3	VIN	P	Main Power Supply (=VIN)
4	SCL	I	I2C clock
5	SYNC	I/O	1.Synchronization pin Open Drain;2. Positive Input of ATOA(I/O)
6	NC	-	No connect
7	SDA	I/O	I2C data
8	GND	P	Supply Ground
9	nINT	O	1.Interrupt or Alarm Out Pin;2. Negative Input of ATOA(O)
10	REG	P	Internal 1.8 V Regulator Output
11	PUMP	P	Internal 2.2 V Regulator Output Analog Power
12	CLK_SYNC	I/O	CLK Synchronization Pin, Can Be Set to Either Master or Slave Mode(I/O)
13	NC	-	No connect
14	NC	-	No connect
15	ADDR	I	IIC Slave Address: Pull Down:7'b1000100; Pull Up:7'b1000101; No connect:7'b1000110
16	SW	P	Internal Power Converter Switch Pin
17	GND	P	Supply Ground
18	GND	P	Supply Ground
19	GND	P	Supply Ground
20	SW	P	Internal Power Converter Switch Pin
21	HV	P	High-Voltage Output
22	HV	P	High-Voltage Output
23	OUT-	P	Negative Differential Output
24	NC	-	No connect
25	GND	P	Supply Ground

(1) Legend: A = Analog Pin; P = Power Pin; D = Digital Pin; I = Input Pin; O = Output Pin.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Min	Max	Unit
Voltage at pins HV, OUT+, OUT-, SW	−0.3	110	V
Voltage at all other pins	−0.3	7	V
Junction temperature	−40	150	°C
Storage temperature	−65	150	°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 4.

Parameters	Min	Typ	Max	Unit
Operating Temperature	−40		125	°C
Continuous Supply Voltage (V_{IN})	2.3		5.5	V
Load Capacitance			1000	nF
Inductance	10	47	68	μH
Output frequency	1		1000	Hz
Junction Temperature (T_J)	−40		125	°C

ELECTROSTATIC DISCHARGE (ESD)

Table 5. ESD Rating

Parameters	Description	Rating	Unit
HBM	Human Body Model ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
CDM	Charged Device Mode ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±500	V
Latch-Up	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±200	mA

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THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 6. Thermal Resistance

Item(1) (2)	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	TBD	°C/W
θ_{JC_Top}	Junction-to-case (top) thermal resistance	TBD	°C/W

(1) The package thermal impedance is calculated in accordance to JESD 51-7.

(2) Thermal Resistances were simulated on a 4-layer, JEDEC board.

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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ELECTRICAL SPECIFICATIONS

V_{IN} = 3.6 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_J = 25°C of AWP1923AA for typical specifications, unless otherwise noted.

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Voltage at REG pin	V_{REG}		1.62	1.80	1.98	V
Digital low-level input voltage	V_{IL}				0.5	V
Digital high-level input voltage	V_{IH}	SDA, SCL, GPIO & SYNC pins	1.26			V
Digital low-level output voltage	V_{OL}				0.4	V
Digital high-level output voltage	V_{OH}		1.26			V
Full-scale output voltage	$V_{OUT(FS)}$		186	190	194	V_{PK_PK}
VIN Quiescent current	I_{Q_VIN}	SHUTDOWN Mode		1.3	2.7	µA
		SLEEP Mode		5	50	µA
		IDLE Mode		90	140	µA
Maximum Inductor Current(1)	I_{L_MAX}			1000		mA
Average VIN supply current during operation(2)	$I_{VIN,AVG}$	V_{IN} = 5 V f_{OUT} = DC V_{OUT} = 95 V C_{LOAD} = 100 nF		14		mA
		V_{IN} = 3.6 V f_{OUT} = 300 Hz V_{OUT} = 190 Vpk-pk C_{LOAD}= 100 nF		127		mA
Total Harmonic Distortion + Noise	THD+N	f_{OUT} = 250 Hz V_{OUT} = 190 Vpk-pk C_{LOAD} = 100 nF		1		%
Programmable FIFO playback rate(1)	fs-FIFO	PLAY_SRATE[15:0]=0x0000	985	1024	1065	ksps
		PLAY_SRATE[15:0]=0xFFFF		0.015		ksps
Piezo Sensing Resolution	PSR	CONFIG.GAINS=0x1		8.8		mV
		CONFIG.GAINS=0x0		46		mV
Start-up Time	tstart	Time from SLEEP mode to haptic waveform playback			200	µs
Sensing Detection to Haptic Feedback Latency	DHL	Time from sensing detection event to automatic playback			30	µs
Full scale input range of ADC(1)		ADC_Gain=0	-0.35		18	V
		ADC_Gain=1	-0.35		100	V
Offset error(3)	ADC V_{OS}		-4	0	4	lsb
Gain error	ADC GE		-1		1	%
Differential nonlinearity	ADC DNL		-1.5		1.5	lsb

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Integral nonlinearity	ADC INL		-2		2	lsb
Effective number of bits	ADC ENOB			10		bit
Offset error(3)	DAC V_{OS}		-1		1	lsb
Gain error	DAC GE	OUT Vpk=190	-1		1	%
Differential nonlinearity	DAC DNL		-0.9		0.9	lsb
Integral nonlinearity	DAC INL		-2.0		2.0	lsb

(1) This parameter is related to the device part. See Ordering Information for more details.

(2) This parameter is strongly correlated to the DCR of the inductor, which was tested on PA4342.473ANLT.

(3) These characteristics is guaranteed by design.

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PACKAGE INFORMATION

PACKAGE TOP MARKING

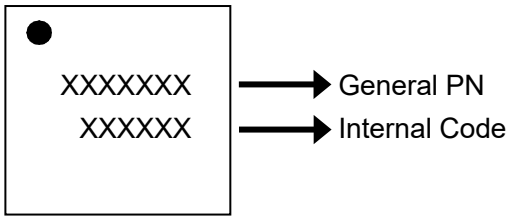

Fig. 4 WLCSP20B Package Top Marking

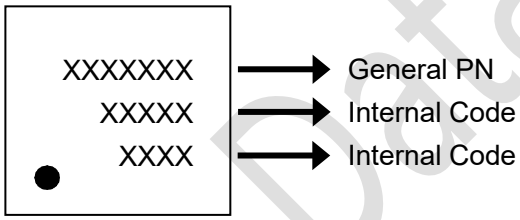

Fig. 5 QFN24L Package Top Marking

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TAPE AND REEL BOX INFORMATION

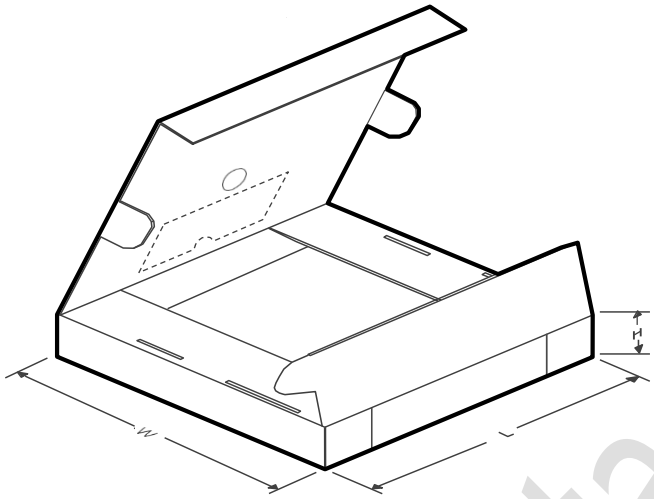

Fig.6 Tape and Reel Box Information

DEVICE	PACKAGE TYPE	PACKAGE DRAWING	PINS	SPQ	LENG (mm)	WIDTH (mm)	HEIGHT (mm)
AWP1923BBR	QFN4*4-24L	BB	24	3000	320.0	320.0	48.0
AWP1923CAR	WLCSP 20B 2.1mm × 1.7mm	CA	20	3000	210.0	210.0	30.0

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TAPE AND REEL INFORMATION

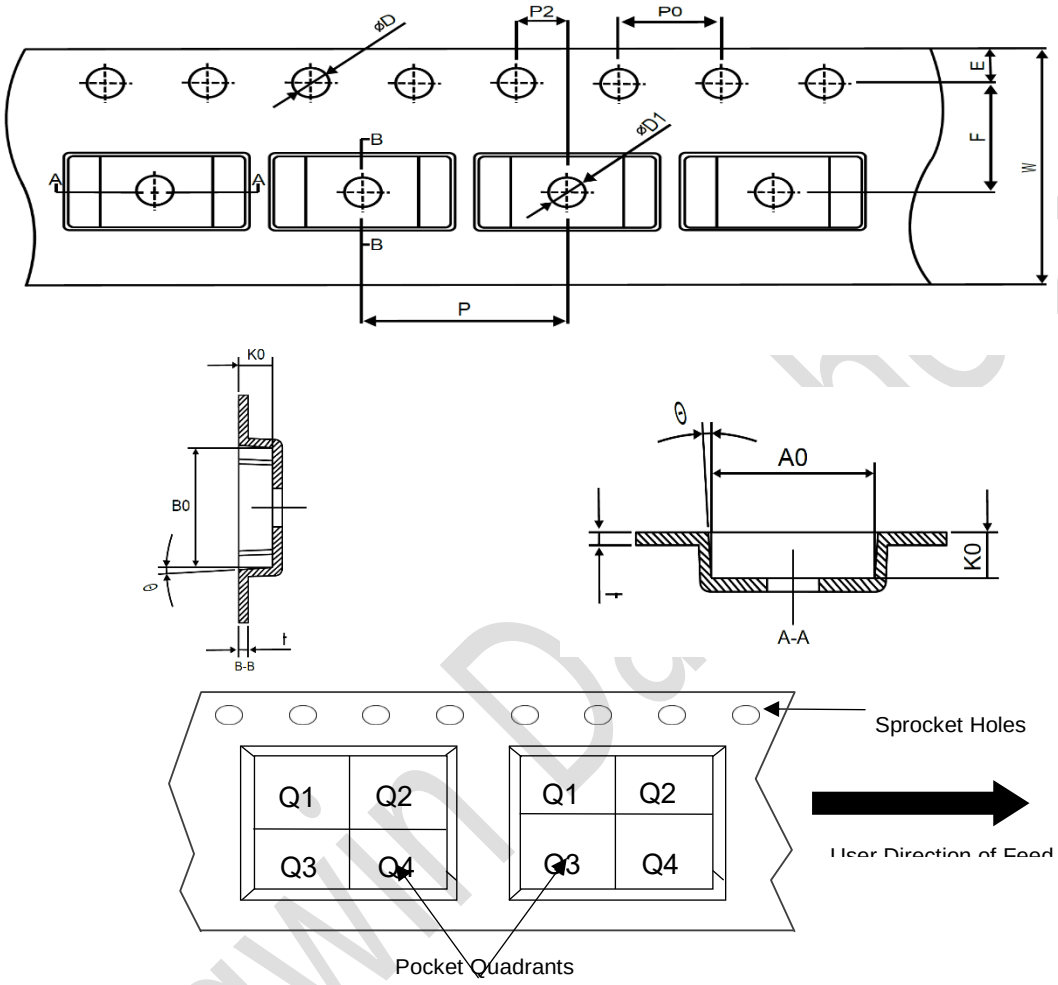

Fig. 7 TAPE and Reel Information

DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W (mm)	Pin1 Quadrant	Quantity
AWP1923BBR	QFN4*4-24L	6.55	5.30	2.00	4.00	12.00	Q1	3000
AWP1923CAR	WLCSP 20B 2.1mm × 1.7mm	1.95	2.3	0.75	4.00	8.00	Q2	3000

All dimensions are nominal

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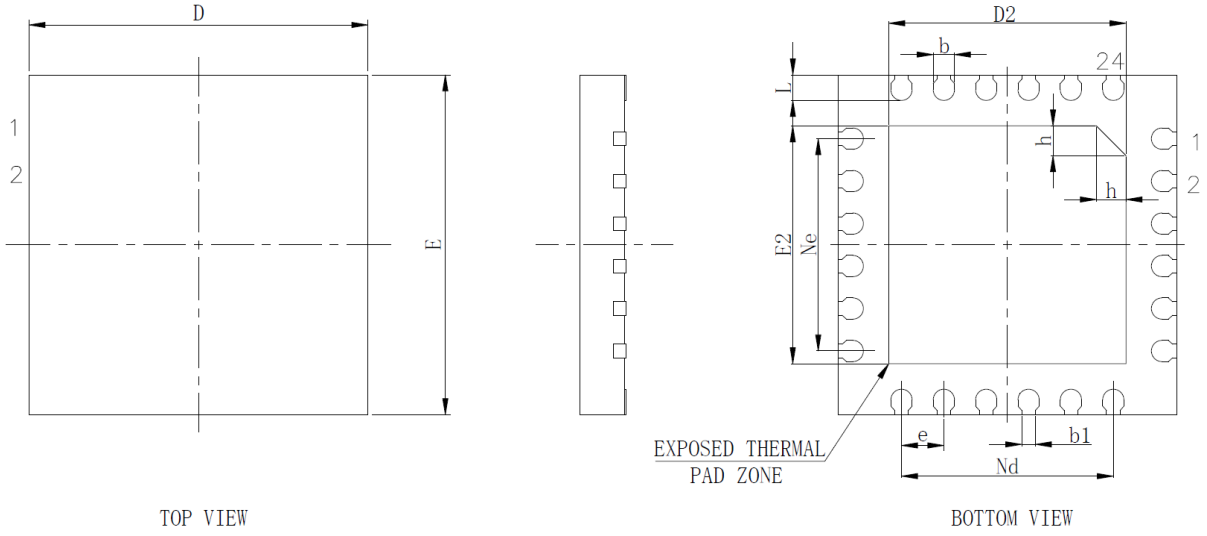
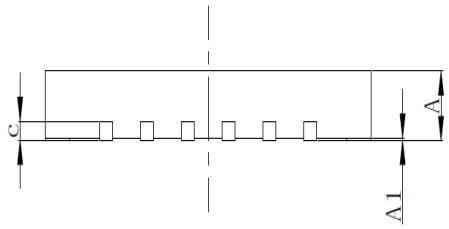
PACKAGE OUTLINES



TOP VIEW

BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.16REF	
c	0.10	0.15	0.20
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40

*Fig 8. QFN4*4-24L PKG*

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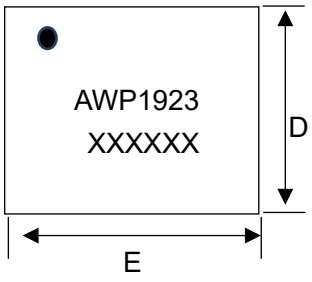
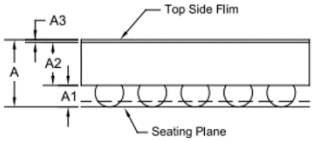
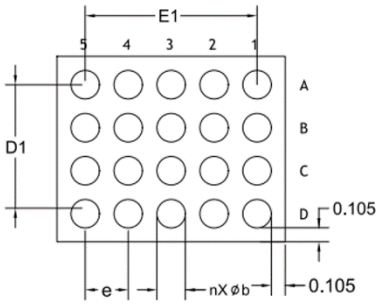
PACKAGE OUTLINES



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.595	0.625	0.655
A1	0.180	0.200	0.220
A2	0.387	0.400	0.413
A3	0.20	0.25	0.30
D1	1.1	1.2	1.3
E1	1.5	1.6	1.7
b	0.245	0.265	0.285
D	1.75	1.77	1.79
E	2.15	2.17	2.19
e	0.4BSC		

Fig 9. WLCSP 20B 2.1mm × 1.7mm PKG

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ORDERING INFORMATION

Device	Order Part No.	Inductor Current	FIFO Frequency	Maximum Output Voltage	Package	QTY
AWP1923	AWP1923AABBR	1000mA	1024	190Vpk-pk	QFN24L, Pb-Free	3000/Reel
	AWP1923AACAR	1000mA	1024	190Vpk-pk	WLCSP 20B Pb-Free	3000/Reel
	AWP1923ABBBR	1600mA	1024	190Vpk-pk	QFN24L, Pb-Free	3000/Reel
	AWP1923ABCAR	1600mA	1024	190Vpk-pk	WLCSP 20B Pb-Free	3000/Reel
	AWP1923ACBBR	800mA	1024	190Vpk-pk	QFN24L, Pb-Free	3000/Reel
	AWP1923ACCAR	800mA	1024	190Vpk-pk	WLCSP 20B Pb-Free	3000/Reel

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REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	07/2024	Initial version

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